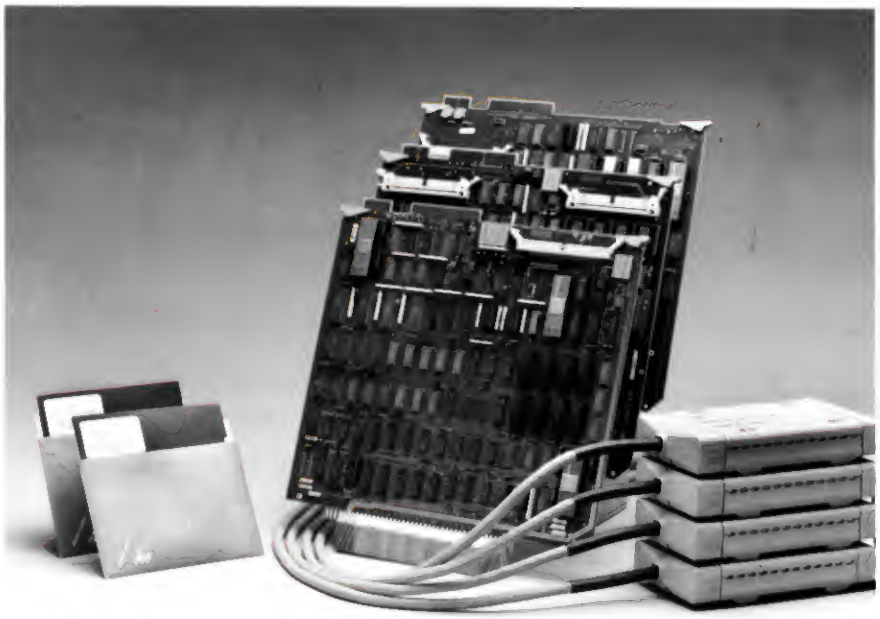
HEWLETT PACKARD

Logic State/Software Analyzer

MODEL 64620S

TECHNICAL DATA 1 DEC 83



Description

Model 64620S Logic State/Software Analyzer adds real-time, nonintrusive software analysis to the HP 64000 Logic Development System. Capable of displaying results in terms of assembly and/or high-level languages, the analyzer is a powerful tool for software analysis, optimization, testing, and performance evaluation. Extensive software performance analysis features nonintrusively provide essential activity information both at the system and procedure levels. A symbolic interface, highly integrated with the software development environment, provides straightforward measurement specification and interpretation.

Nonintrusive analysis of programs written in high-level languages is facilitated by the instrument's ability to display measurement traces in terms of high-level statements along with associated comment lines. As part of the HP 64000 Development System, the HP 64620S is capable of tracing both Pascal and C, along with assembly-level languages. Use of the HP 64620S language analysis capability is not limited to code generated by the HP 64000 Development System. With minimum effort, Model 64620S analyzer can perform high-level language analysis on code developed on other software development systems. A mixed display, showing high-level statements combined with the resulting assembly-level execution aids in optimization and debug efforts, and is similar in appearance to an expanded compiler listing. An assembly-level-only display is available as well.

Features

- Real-time, nonintrusive analysis for high-level or assembly language programs speeds software debugging
- Separate trigger, store, and count functions combined with powerful sequencing and windowing capability allow precise isolation of the area program to be analyzed
- Software performance measurements coupled to trace measurements provide new dimensions to software analysis
- Variety of probing schemes to fit various target system requirements
- Configurable as a portable, stand-alone instrument
- Interactive with other 64000 analysis and emulation subsystems
- Command file execution during analysis speeds measurement set-up and execution and facilitates automatic measurements
- Configuration files for repetitive measurements and rapid recall of previous measurements

A close link to the 64000 software development environment provides an extensive symbolic interface to the analyzer. Programmers can specify measurements and interpret their results using actual procedure, symbol, and file names, along with source file line numbers. To capture and analyze program segments, such as I/O sequences, the powerful trigger features of the 64620S analyzer pinpoint program activity. Separate data storage controls capture only the data of interest. Counting functions allow state-to-state timing or event counting, and provide yet another dimension to software analysis. A 15-level sequencer expands the capability to the trigger, store, and count functions, providing advanced measurement qualification.

Model 64620S Analyzer also incorporates software performance analysis features. Performance analysis uses dynamic histograms, graphs, or tabular displays to locate throughput bottlenecks and spot areas where optimization efforts will be most beneficial. Since trace analysis and performance analysis are independent functions of the HP 64620S, they can be used interactively. The trace analyzer, for example, may be triggered when excessive time is spent executing a particular subroutine. Information gained from such measurements can isolate causes of improper parameter values, or point out inefficient algorithms.

HP 64620S Analyzer may be configured from 20 to 120 channels, in 20 and 40 channel increments. Three probing techniques provide flexible, yet simple, connections to the target system. The HP 64620S may be connected to the target system via General Purpose Probes, or may monitor the CPU through the HP 64650A General Purpose Preprocessor and associated processor-specific interface modules. When used in an emulation environment, the analyzer may be internally connected directly to the HP 64000 emulation bus via Model 64304A Emulation Bus Preprocessor. The instrument may be operated as part of a 64000 system cluster, or can be installed in a portable station (HP 64110A) for stand-alone benchtop use.

Logic State/Software Analyzer Architecture

Model 64620S may be configured for between 20 and 120 channels, using a control card and from one to three data acquisition cards. Two types of acquisition cards are available: the 20-channel card, which includes the software performance features, and the 40-channel card. The table illustrates the various possible analyzer configurations. Note that the software performance features are available only in configurations using a 20-channel acquisition card.

Number of Input Channels	Control Cards	20-Channel Cards	40-Channel Cards	Software Performance Features
20	1	1	0	yes
40	1	0	1	no
60	1	1	1	yes
80	1	0	2	no
100	1	1	2	yes
120	1	0	3	no

Format Specification

The Format Specification establishes the conditions and relationships of target system signals transmitted to the analyzer through the clock and data input circuits (figure 1).

Here, an input channel, or a contiguous group of channels, may be assigned a user-defined label. If, for example, the CPU address lines are brought into the analyzer on Data Pod 1, channels 0 through 15, the label "ADDRESS" could be assigned to that group of input channels, with other labels assigned to CPU data, status, etc., channels. Sixteen-character labels may be assigned to signal groups from one to 32 channels wide. Once a label is assigned to a group of input channels, it then appears on the analyzer softkeys, minimizing the amount of typing necessary to specify a given measurement. This association allows for rapid and convenient measurement setup and interpretation of results.

To avoid confusion caused when both negative- and positive-true data is present in the system under test, Model 64620S can automatically complement any group of data channels. This relieves the user from unnecessarily having to invert these signals on the target system, or tediously complement data as measurements are specified or their results interpreted.

The positive and/or negative going edges of up to eight separate clock signals may be used to capture data. This multiple clock capability makes it possible to analyze systems with multiple CPU's by capturing data on each processor's address strobe signal. Additional clock qualifier lines may be used to further qualify the system clock to capture specific CPU cycles — DMA cycles for example. These qualifier lines may be used to capture data from systems with up to a 25 MHz bus cycle rate, as long as the actual storage rate of the HP 64620S does not exceed 10 MHz.

Data and clock signal switching threshold voltages may also be varied. Proper thresholds for TTL and ECL logic families have been preprogrammed, but is also possible to select other values between -10 and +10 volts, in 100 mV increments. A choice of threshold values is essential when monitoring a system composed of several different logic families. Independent threshold specifications may be made for each data pod. The eight clock channels are divided into two groups of four channels, with independent threshold settings for each group.

A dynamically updated channel activity display immediately indicates the current data or clock channel levels. This aids in making the proper analysis connections, and immediately indicates the possibility of open, intermittent, or shorted target system signals.

The analyzer Format Specification is permanently stored when the analyzer configuration file is saved. This provides rapid measurement setups by removing the necessity to respecify data channel labels, threshold levels, and clock characteristics, each time the analyzer is used. This is particularly beneficial for performing automatic tests, or when recalling previous measurements. The Format Specification is automatically set up for the appropriate CPU when Model 64620S Logic/State Software Analyzer is used in conjunction with Model 64650A General Purpose Preprocessor or Model 64304A Emulation Bus Preprocessor.

Map Specification

The Map Specification provides for the association of captured data with user-defined symbols, assisting in measurement specification and interpretation (figure 2).

A "symbol map" may be associated with any labeled input channel(s). The use of a symbol map allows captured data values to be displayed or referred to in terms of user-defined symbols. Entries in a symbol map appear as part of the analyzer softkey syntax and provide rapid measurement set-up. These symbols may also appear in the displays of measurement results.

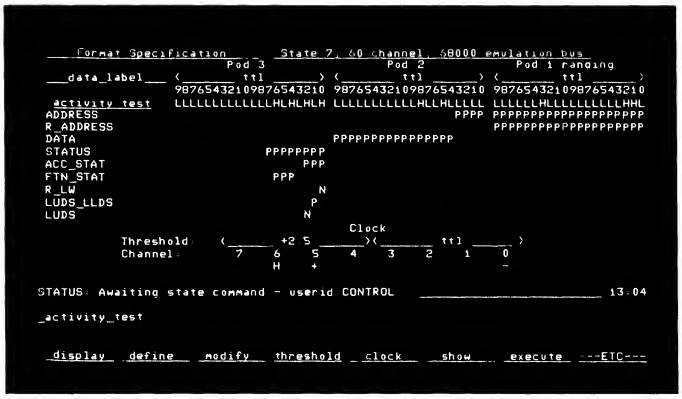


Figure 1. The Format Specification showing user-defined labels assigned to data input channels, a clock specification, with thresholds, and the dynamic activity display.

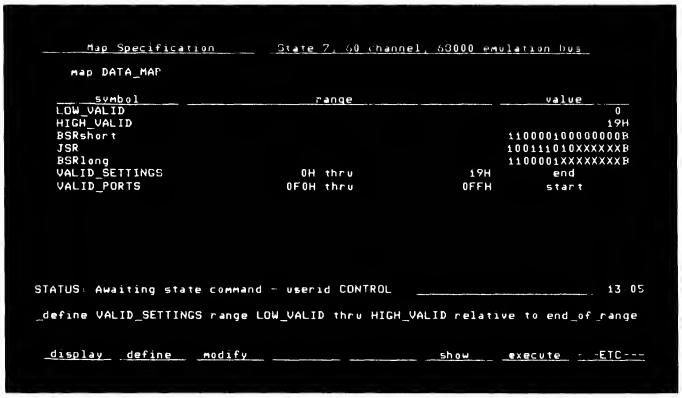


Figure 2. Map Specification showing symbol map DATA_MAP. This map can be associated with the analyzer input channels labeled DATA.

The definition of such symbols may use file, procedure, and function names, along with source file line numbers. Constants, ranges and "don't care" terms may also be used.

Trace Specification

Trigger

The trigger function determines WHEN the analyzer will capture data. Complex triggering conditions can be implemented with up to eight ORed trigger patterns (figure 3). These patterns may include symbolic or absolute values, ranges, "don't care" terms, and NOT terms. File, procedure, and symbol names, in addition to source file line numbers, may also be used to specify trigger conditions. Other 64000 analysis modules may be used to directly trigger the instrument.

Further, the position of the trigger state within the analyzer trace may be specified, producing measurements after, surrounding, or before the trigger condition is encountered.

A hierarchial "trigger enable" function creates an "arming" function, enabling or disabling trigger recognition.

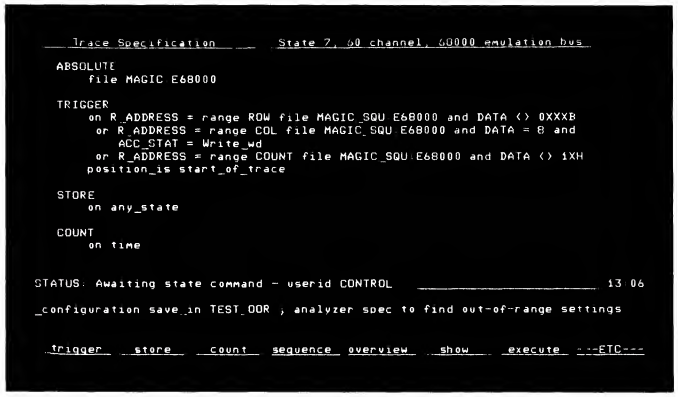


Figure 3. Trace specification with three ORed terms used to define the trigger condition.

Store

The store function determines WHAT data should be stored (figure 4). The options for specifying types of states to be stored are the same as those used to specify the trigger point. The storage qualification technique, resulting from separate trigger and store functions, is extremely valuable for filtering irrelevant data from measurement results. Like the trigger function, storage may be "enabled always" or can be controlled by the sequencer, windows, or other analysis modules.

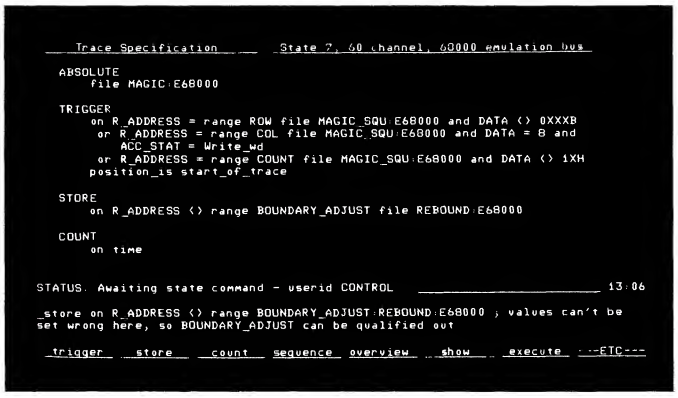


Figure 4. Trace Specification with trigger and store conditions specified. The "< >" symbol indicates "not equal to."

Count

The count function measures the amount of activity between stored states, or between the trigger point and each stored state (figure 5). Activity between stored states may be indicated by time measurement, or by a count of the number of states meeting specific conditions that occurred between the stored states. This is extremely significant, for example, in counting the number of interrupts occurring during the execution of a specific procedure and estimating the associated impact on system performance. A typical application uses the count function to total the number of disc accesses during a sorting procedure and uses this data to evaluate the effectiveness of sorting algorithms.

The maximum time count is 8.3 hours with a resolution of 40 ns or 0.1%, whichever is greater. Up to four patterns, like those used for trigger and store, may be used to designate the characteristics of the state(s) to be counted. The "count enable" function may be controlled by the sequencer or by either window.

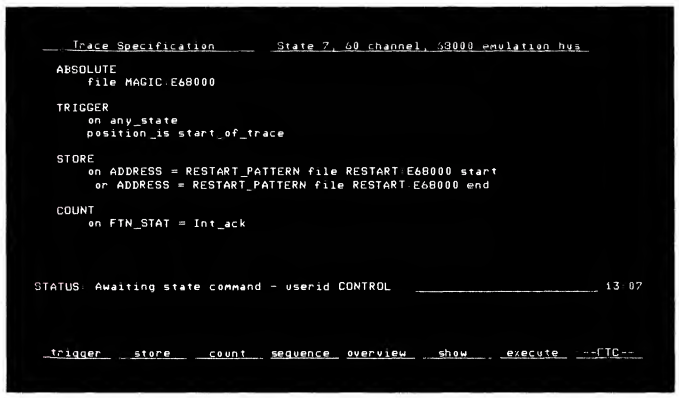


Figure 5. Trace Specification whose count function determines the number of interrupts during the execution of subroutine RESTART_PATTERN.

Sequencer

The sequencer allows the associated trigger, store, count, or overview functions to be simultaneously or separately controlled. The sequencer may be directed to control the "enable" portion of trigger, store, count, or overview, acting as an arming control for that particular function. Each sequencer term may carry an optional modifier, causing the associated function(s) to be enabled and disabled appropriately as specific sequence events are recognized.

Additionally, specific sequence terms may be directed to actually trigger the analyzer, or to cause a state to be stored or counted. This is especially useful when using the sequencer to detect the occurrence of a complex procedure flow. For example, subroutine INPUT may function precisely as intended, unless preceeded in execution by procedures TEST, PREPARE, and LOG, in that order. Here, the sequencer can be directed to follow the procedure flow, and trigger the analyzer only if INPUT is executed in the prescribed order (figure 6).

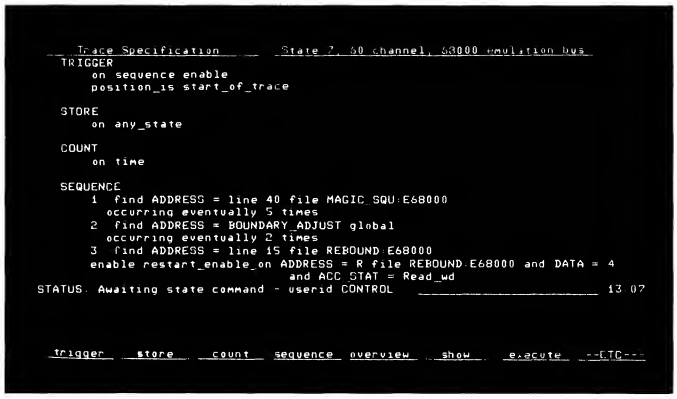


Figure 6. Powerful sequencing capabilities direct analysis to the areas of interest.

Up to 15 sequencer terms may be defined using symbolic or absolute values, symbol, procedure or file names, "don't care", and NOT terms. During normal operation, each sequencer term must be satisfied before the "search" for the next term may begin. Such a term may be a single pattern or logical combination of patterns, specified to occur 1 or N times before that term is satisfied. In this way, the sequencer term could be satisfied only on the 12th iteration of a loop, or the 9th access to a specific I/O port.

The sequencer may be programmed to find events immediately following one another, or may be defined to find an event occurring at any time after the preceeding event. It is also possible to cause the sequencer to completely restart, or to return to a previous point when a "restart" event is encountered before a given sequencer term is satisfied.

Windows

A window is used to recognize a specific analysis context (figure 7). It may, for example, be used to determine when a specific overlay is executing, and enable the trigger, store, count, and/or overview functions appropriately. This allows analysis of various program segments only when they are operating in a desired context.

Each of the two windows are defined as an enable/disable pair. Related functions are enabled between the appropriate window enable and disable terms, and are disabled otherwise.

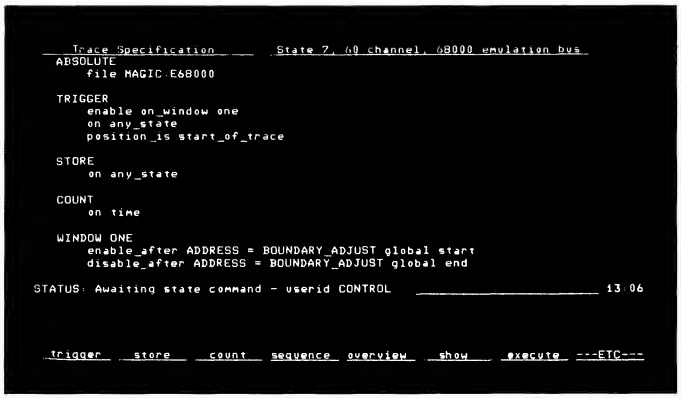


Figure 7. Trace Specification showing a window being used to detect execution within a specific procedure.

A window and sequencer resources are shared, the number of windows in use affects the number of sequencer terms available according to the following table:

Number of Windows in Use	Number of Sequencer Terms Available
0	15
1	7
2	3

Master Enable

The Master Enable function is responsible for enabling all analysis functions (figure 8). While false, all analysis activity ceases until the enabling condition again becomes true. The Master Enable function can be controlled by the sequencer and windows, and may be controlled from another analysis module. This function is of particular interest when monitoring execution in a multiprocessing environment, where a task may be suspended, or swapped out of memory before it has completed. By judicious use of the Master Enable function, the analyzer can be directed to suspend its operation until the task is once again reinstated.

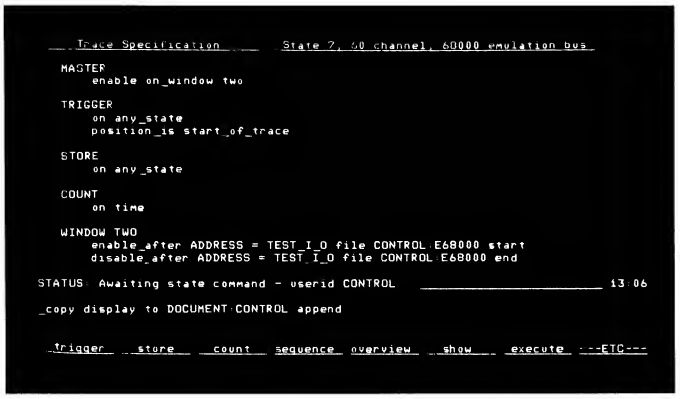


Figure 8. A Master Enable specification allowing analyzer operation only while procedure TEST_I_O is executing.

Overview Mode for Software Performance Analysis

When configured with an HP 64623A 20-Channel Data Acquisition Card, powerful software performance analysis features become an integral part of the Logic State/Software Analyzer. This measurement capability provides essential information allowing precise evaluation of system performance (figure 9). Such measurements are beneficial in locating throughput bottlenecks, evaluating effectiveness of algorithms, and for determining areas where optimization efforts will be most beneficial.

A 4096-state memory, resident on the 20-Channel Data Acquisition card, logs specific occurrences, counts time, or counts states. For every 4096 occurrences logged, a real-time picture of the activity relating to each defined overview event is displayed as a bar graph (histogram), an event graph, or an event list.

The trace capability and overview functions are separate functions of the analyzer. As such, the trace analyzer can be triggered, for example, when a module exceeds its normal execution time. Such a measurement can isolate causes of improper algorithm execution, or spurious parameter values.

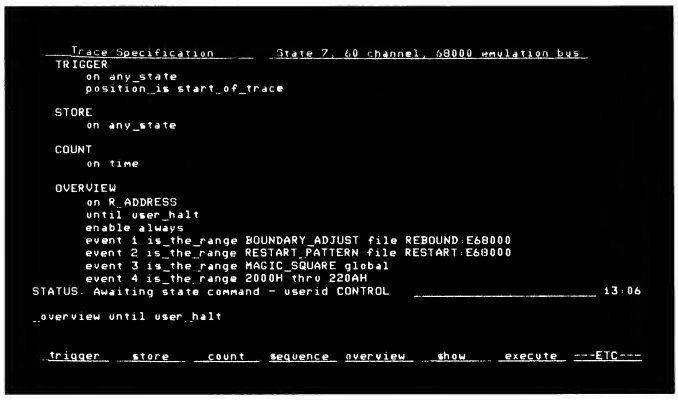


Figure 9. Overview events are specified within the Trace Specification, and may include symbols from symbol maps, or from program files.

Acquired overview data may be displayed in several forms. In the histogram mode, the X-axis represents an occurrence percentage, relative to the other overview events and/or other system activity (figure 10). The X-axis may be specified to dynamically rescale itself so that the event with the largest occurrence percentage is displayed full scale.

Figure 10. Overview information displayed in histogram form permits easy interpretation of system activity.

An alternate overview display, the overview graph shows the sequence of occurrence of the captured overview events (figure 11). Here as well, the X-axis may be rescaled to focus on any area of interest. Information may also be displayed as a table (figure 12).

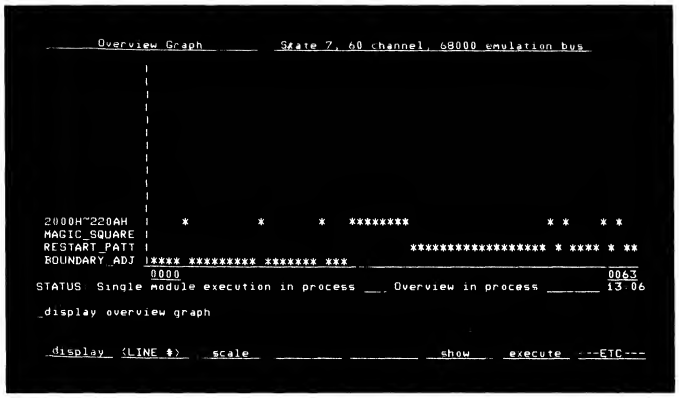


Figure 11. The sequential order of overview events is pictorially represented in the graph mode.

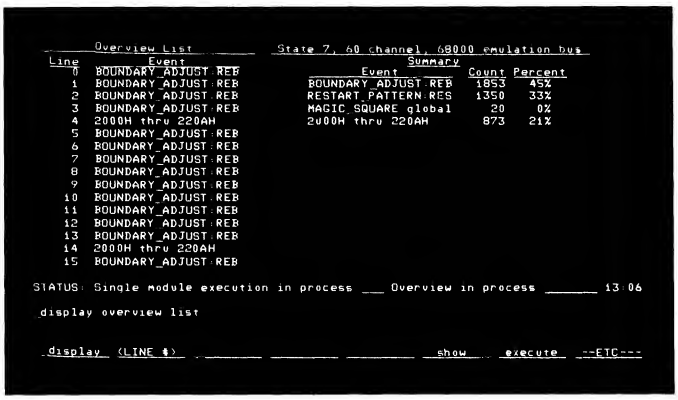


Figure 12. A tabular representation, the overview list also presents the order of occurrence of overview events.

Interval Overview

Monitoring time duration, or state count activity of a particular procedure or other program area is accomplished by defining appropriate overview start and stop conditions. Such a measurement is useful for making time distribution measurements of particular procedures, functions, or other program areas (figure 13). Through histograms, measurement results indicate maximum, nominal, and minimum execution times, and lead to thorough understanding and characterization of system software. Up to 15 time intervals may be defined within 40 ns or 0.1% (whichever is greater) resolution.

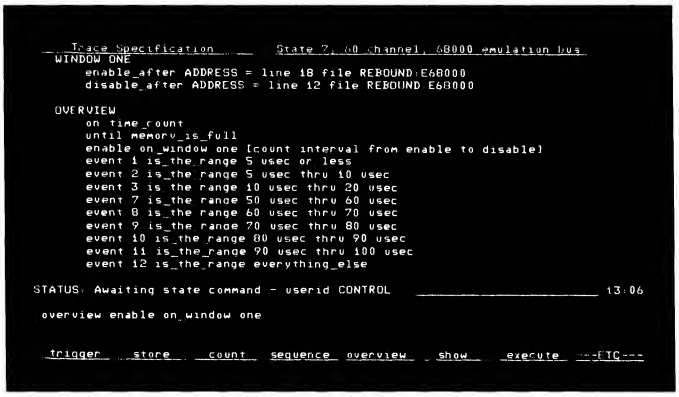


Figure 13. Time interval overview specification sets up a series of time invervals and defines a code segment to be analyzed with respect to execution times.

The time interval overview mode measures the percentage of executions within a given time interval, and compares this to execution within other time intervals (figure 14).

Figure 14. Interval overview allows rapid detection of spurious execution times, and is a powerful software characterization technique.

Similar interval measurements count the number of bus cycles occurring within the designated interval. This measurement renders information concerning algorithm or subroutine impact on overall system performance from a bus utilization standpoint.

Measurement Results

Analyzer measurement results may be displayed in terms of high-level languages. As the analyzer is part of the HP 64000 Logic Development System, it is capable of tracing programs written in Pascal and C (figure 15). In addition to the high-level statements themselves, appropriate file names, line numbers, and associated comments are also displayed. With minimal effort, this analysis capability can be directed to programs written in high-level languages employed by other software development systems.

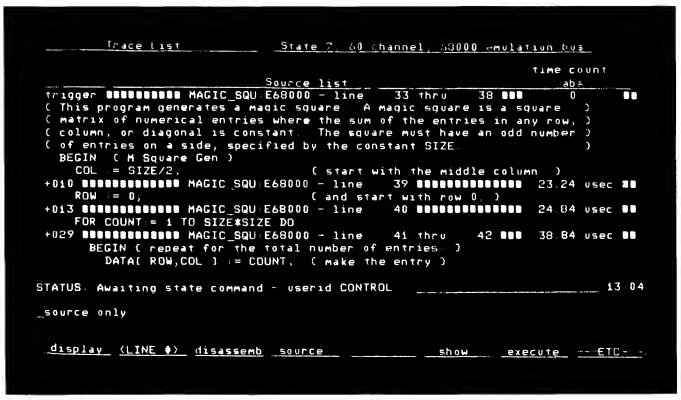


Figure 15. High-level language tracing of a program written in Pascal.

Resembling an expanded compiler listing in appearance, a mixed display shows high-level statements combined with the resulting assembly-level execution (figure 16). Powerful inverse assemblers display execution in the assembly language of the processor being monitored (figure 17). These displays also include user-defined symbols specified in the symbol maps, and may as well automatically reference external symbol tables generated during software development.

Figure 16. Mixed mode display showing high-level C source lines, combined with inverse assembly and symbolic tracing.

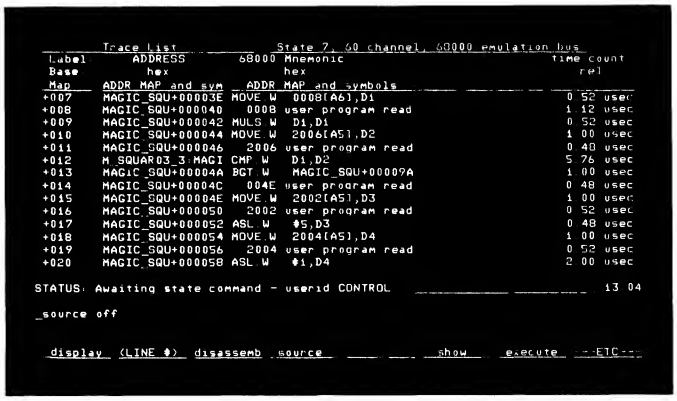


Figure 17. Assembly-level display with symbolic tracing.

Measurements Involving Multiple Analyzers

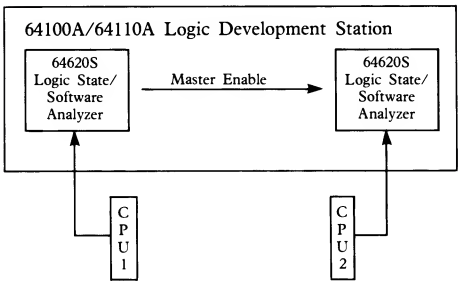
Interactive measurements involving two or more 64000 analysis modules are extremely useful in tracking hardware/software, software/software, and hardware/hardware interaction problems. Supervised and controlled on a global level by the 64000 Measurement System, these measurements are conducted via the high-speed Intermodule Bus (IMB). The IMB carries signals between analysis subsystems, providing extensive and advanced measurement capability. Subsystems that may operate interactively include:

64620S Logic State/Software Analyzer
64600S Logic Timing/Hardware Analyzer
64310A Software Performance Analyzer
64302A Emulation Bus Logic Analyzer
64300A Emulation Bus Logic Analyzer
64XXXS Emulation Subystems

The 64620S Logic State/Software Analyzer interacts with other analysis subsystems with the five IMB signals shown below:

IMB Signal Name	Received by 64620S	Driven by 64620S
Master Enable	yes	yes
Trigger Enable	yes	yes
Trigger	yes	yes
Storage Enable	yes	yes
Delay Clock	no	yes

The Master Enable signal coordinates measurement starts with other analyzers and emulators. Furthermore, when the analyzer is specified to receive this signal, and master enable is "false", the analyzer is completely disabled and will not capture information. When Master Enable again becomes "true," the analyzer will resume examining data. In this way, the Master Enable signal functions as a high priority "window," allowing data capture at some times, and disabling it at other times. An application illustrates the analysis power derived from such capability. In a multiple CPU environment, one Logic State/Software Analyzer, monitoring CPU #1 can use Master Enable to control the data acquisition of a second HP 64620S monitoring CPU #2. In this case, an important subroutine executing on CPU #2 may fail only while CPU #1 is attempting to establish a communications link through CPU #2. Here, the analyzer monitoring CPU #1 can use the Master Enable signal to cause the analyzer for CPU #2 to be active only while the link is being established. This causes the analyzer for CPU #2 to look for aberrant subroutine conditions only when applicable.



The Trigger Enable signal functions in much the same way as Master Enable, in that it informs the receiving analysis module when it may recognize its trigger condition. It functions, therefore, as an "arming" control.

The Trigger signal, when received, causes the analyzer to immediately trigger, and subsequently complete its measurement. This is of value, for example, when using Model 64600S Logic Timing/Hardware Analyzer in conjunction with a Logic State/Software Analyzer to determine if a spurious signal pulse may be related to a software event. Here, the Logic Timing/Hardware Analyzer is directed to trigger on the occurrence of the spurious pulse, with the Logic State/Software analyzer set to receive the trigger signal. Triggering essentially on a hardware event, the HP 64620S then displays the software flow surrounding the suspicious signal pulse. By this means, the software responsible for initiating the pulse can be quickly and methodically pinpointed.

The Storage Enable signal may be received or driven by the HP 64620S. It is responsible for exercising a hierarchial control over the store specification, similar to the way in which Trigger Enable has precedence over Trigger.

Multiple analyzer measurements using these techniques, are extremely advantageous in relating software execution to various other software and hardware events. Multiple subsystem measurements extend the capabilities of analysis modules, and when performed with the Model 64620S Logic State/Software Analyzer, provide alternative, enhanced views as to the hardware or software conditions responsible for unexpected deviations. This information is beneficial in carrying out accurate and rapid characterization of such problems and directs engineers to efficient and correct solutions.

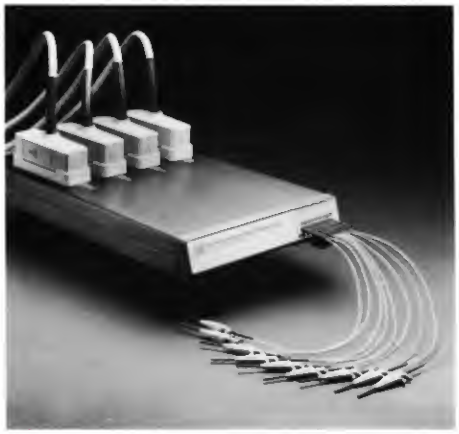
Flexible Probing Capability

Model 64630S General Purpose Probes

General Purpose Probes provide the highest degree of probing flexibility and are suitable in a variety of environments. With this probing scheme, wire probe leads may be connected to virtually any point in the target system. Alternatively, a 25-pin D-type connector may be used to interface the probes to an "analysis port" that may be a permanent part of the target system. To detect the logic state of the incoming signals, the probes are analyzer-programmable with signal-switching threshold voltages from -10 to +10 volts in 100 mV increments.

Model 64650A General Purpose Preprocessor

The General Purpose Preprocessor provides a dedicated, microprocessor-specific interface from the target system to the analyzer. Used in conjuntion with the General Purpose Preprocessor, processor-specific Interface Modules provide a simple and compact connection to the target system microprocessor. An identification code, available to the analyzer from each interface module, informs the analyzer as to the type of microprocessor being monitored, and initiates automatic analyzer configuration. This causes the analyzer to appear as if it were specifically designed for the microprocessor under test.



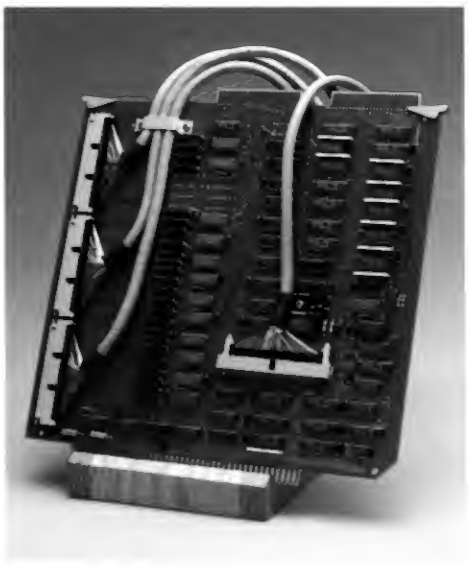
Signal switching thresholds, to differentiate between high and low logic levels, may be programmed by the analyzer. In addition, this preprocessor is capable of real-time demultiplexing of up to 32 of its 60 input channels. This furthers nonintrusive analysis by eliminating the need to perform analysis-specific functions on the target system.

Several nondedicated input/output lines may be used to perform user-defined functions. The halt and stimulus signals from the analyzer may be used to interrupt or halt the processor under test, dependent, for example, upon the occurrence of a specific sequence of events. Unused input channels provide for the analysis of other target system signals of interest.

A User-Definable Interface kit, and the User-Definable Inverse Assembler combine to enable the user to create a convenient, processor-specific interface for microprocessors not currently supported by Hewlett-Packard.

Model 64304A
Emulation Bus Preprocessor

The Emulation Bus Preprocessor provides a powerful and convenient interface between the HP 64000 emulation environment and the Logic State/Software Analyzer. This single card preprocessor plugs into the development station along with the emulation subsystem. The Logic State/Software Analyzer may be resident in the same station, or can be located in another station. As this preprocessor allows the Analyzer to monitor the emulation bus directly, it has access to all memory activity, including internal emulation and external user memory references. This HP 64304A directs the powerful and sophisticated measurement capability of the HP 64620S to the emulation environment.



The Emulation Bus Preprocessor allows the Logic State/Software Analyzer to assert a break condition on executing emulation software. The break condition may be a simple address, or may be an extremely complex event as defined by the sequencer and/or windows.

Accessories Supplied
Model 64620S
Logic State/Software Analyzer

In addition to the circuit cards and cables listed in the table, each Model 64620S Logic State/Software Analyzer is supplied with the following accessories: one Clock Cable (P/N 64620-61602), Operating Software on Flexible Disc, and Operating and Service Manuals.

Model Number	64621A Control Cards	64622A 40-Chan Cards	64623A 20-Chan Cards	64620-61601 20-Chan Data Cables	State Bus Cable
64620S	1	0	1	1	2 pos (P/N 8120-4086)
64620S opt 010	1	1	0	2	2 pos (P/N 8120-4086)
64620S opt 011	1	1	1	3	3 pos (P/N 8120-4087)
64620S opt 012	1	2	0	4	3 pos (P/N 8120-4087)
64620S opt 013	1	2	1	5	4 pos (P/N 8120-4088)
64620S opt 014	1	3	0	6	4 pos (P/N 8120-4088)

Model 64630S
General Purpose Probes

In addition to the HP 64635A Data probes listed in the table, each HP 64630S Logic State/Software Analyzer Probe Set is supplied with one Model 64636A 8-Channel Clock Probe and applicable service manuals.

Model Number	64635A 20-Channel Data Probes
64630S	1
64630S option 010	2
64630S option 011	3
64630S option 012	4
64630S option 013	5
64630S option 014	6

Each Model 64635A 20-Channel Data Probe is supplied with the following accessories: one 21-Lead Wire Assembly (P/N 64635-61602), 21 IC Probe Tip Adapters (P/N 10230-62101).

Each Model 64636A 8-Channel Clock Probe is supplied with the following accessories: one 9-Lead Wire Assembly (P/N 64636-61602), 9 IC Probe Tip Adapters Adapters(P/N 10230-62101).

Model 64650A
General Purpose Preprocessor

Each HP 64650A General Purpose Preprocessor is supplied with the following accessories: ten Probe Leads, ten IC Probe Tip Adapters (P/N 10230-62101), and Operating and Service Manuals.

Model 64304A
Emulation Bus Preprocessor

The following accessories are supplied with each Model 64304A Emulation Bus Preprocessor: one Clock Cable (P/N 64304-61601); three Data Cables (P/N 64304-61603); Performance Verification, Inverse Assembly, and Configuration Software on Flexible Disc; and Operating and Service Manuals.

Specifications

These specifications apply to Model 64620S Logic State/Software Analyzer when operated in the 60-channel configuration consisting of the following equipment:

64621A Logic State/Software Analyzer control card
64622A 40-channel Data Acquisition control card
64623A 20-channel Data Acquisition card
64635A Data Probe (quantity 3)
64636A Clock Probe

CLOCK INPUTS

Clock Channels: 8 edge-sensitive ORed clocks and/or level-sensitive qualifiers.

64636A Clock Probe Specifications
Resistance: approx 100 kΩ.
Capacitance: approx 10 pF at probe lead tips.
Input voltage: -40 Vdc to +40 Vdc.
Dynamic voltage range: threshold voltage, ±10 Vdc.
Thresholds: software programmable from -10 Vdc to +10 Vdc in 100 mV increments.
Unqualified clock rate: up to 25 MHz.
Qualified clock rate: up to 10 MHz.
Clock pulse width: 20 ns minimum.
Clock qualifier setup time: clock qualifier must be present at least 20 ns prior to active clock edge.
Clock qualifier hold time: zero.

DATA INPUTS

Data channels: 20 to 120 input channels (20 channels per 64635A data probe).

64635A Data Probe Specifications
Resistance: approx 100 kΩ.
Capacitance: approx 14 pF at probe lead tips.
Input voltage: -40 Vdc to +40 Vdc.
Dynamic voltage range: threshold voltage ±10 Vdc.
Thresholds: software programmable from -10 Vdc to +10 Vdc in 100 mV increments.
Data setup time: valid data must be present at least 30 ns prior to the active clock edge.
Data hold time: zero.

ANALYZER OUTPUTS

(Output signals are available at the BNC connectors on the rear panel of the Logic Development Station. Specifications are applicable with a 50 Ω signal load.)

BNC Port 1 (Stimulus Signal)
General signal characteristics: TTL pulse with programmable polarity.
When programmed for pulse on trigger events
Pulse width: 50 ns ± 20 ns.
Delay from clock: 225 ns ± 20 ns.
When programmed for pulse on sequencer events
Pulse width: 50 ns ± 20 ns.
Delay from clock: 200 ns ± 25 ns.

BNC Port 2 (Halt Signal)
General signal characteristics: TTL level with programmable polarity.
When programmed for false-to-true transition on trigger
Delay from clock: 225 ns ± 20 ns.
When programmed for false-to-true transition on measurement complete
Delay from clock: 225 ns ± 25 ns.

MEASUREMENT FUNCTIONS

State Analysis

Memory Size
Width: Configurable from 20 to 120 channels.
Depth: 256 states.
Analysis Functions
Note: A total of 8 ORed patterns may be specified for trigger, store and count functions. A total of 4 ORed ranges may be specified when the analyzer configuration contains a 64623A.
Trigger: Up to 8 ORed patterns. Up to 4 ORed ranges when used with HP 64623A.
Store: Up to 8 ORed patterns. Up to 4 ORed ranges when used with HP 64623A.
Count: Up to 4 ORed patterns. Up to 2 ORed ranges when used with HP 64623A.
Time Count: 8.3 hours maximum time, within 40 ns or 0.1%, whichever is greater.
Event Count: From 0 to 611 670 events with one count resolution. Maximum count 750 x 10^9.
Sequence: 15-term sequencer with restart terms. Configurable as a 15-term sequencer with one restart term for each enable or disable term; as a 7-term sequencer with one restart term for each enable or disable term and one window; as a 3-term sequencer with one restart term for each enable or disable term and two windows. Can be used to control trigger, store, count, and/or overview functions.
Master Enable: Enables the entire analyzer. Controlled by the sequencer, windows, or another analyzer. Can be used to control other analyzers.
Software Performance Analysis (Overview)
Note: Software performance analysis is available only in analyzer configurations containing an HP 64623A 20-Channel Data Acquisition Card.
Memory Size
Depth: 4096 events.
Ranging: 20-bit range or a contiguous subset of the 20 ranging bits in the lower 20 input channels.
Control: Sequencer or window controlled.
Operating Modes
Address Data: Up to 15 user-defined overview events.
Time Interval: 8.0 hours within 40 ns or 0.1% whichever is greater.
State Interval: 0 to 611 670 with one count resolution. Maximum count 721 x 10^9.
Overview Displays: Histogram, graph, or tabular list.

ENVIRONMENTAL

Analyzer Cards
Conforms to environmental specifications of Model 64100A or 64110A Logic Development Stations.

Probes
Temperature: 0° C to +55° C (+32° F to +131° F).
Humidity: up to 95% RH at +40° C, noncondensing.
Altitude: up to 4600 m (15 000 ft).

POWER REQUIREMENTS

Current required for the Logic State/Software Analyzer Components.

Note: Refer to the HP 64000 Logic Development System Selection and Configuration Guide for power requirements. The chapter on Configuration Requirements contains data for calculating current required for subsystems to be installed, and currents available in development stations. Model 64100A Development Station, serial number prefix 2136 and below, can be retrofitted to accommodate new subsystems if required. Please contact your Hewlett-Packard Logic Systems Field Engineer for further information.

Model Number	Description	Card Slots	+5 V	-5 V
64620S	20-channels w/overview	2	5.2 A	7.2 A
64620S option 010	40-channels	2	7.0 A	6.3 A
64620S option 011	60-channels w/overview	3	10.4 A	8.8 A
64620S option 012	80-channels	3	12.2 A	7.9 A
64620S option 013	100-channels w/overview	4	15.6 A	10.4 A
64620S option 014	120-channels	4	17.4 A	9.5 A
64630S	20-channels probes w/clock	0	0.2 A	0.6 A
64630S option 010	40-channels probes w/clock	0	0.3 A	1.0 A
64630S option 011	60-channels probes w/clock	0	0.5 A	1.3 A
64630S option 012	80-channels probes w/clock	0	0.6 A	1.7 A
64630S option 013	100-channels probes w/clock	0	0.8 A	2.0 A
64630S option 014	120-channels probes w/clock	0	0.9 A	2.4 A
64621A	Analyzer Control Card	1	1.8 A	4.7 A
64622A	40-channel Data Acquistion	1	5.2 A	1.6 A
64623A	20-channel Data Acquistion	1	3.4 A	2.5 A
64635A	20-channel Data Probe	0	0.1 A	0.4 A
64636A	8-channel Clock Probe	0	0.1 A	0.3 A

Ordering Information

Model 64620S 20-channel Logic State/Software Analyzer (with overview)
Model 64620S Option 010: 40-channel Logic State/Software Analyzer (without overview)
Model 64620S Option 011: 60-channel Logic State/Software Analyzer (with overview)
Model 64620S Option 012: 80-channel Logic State/Software Analyzer (without overview)
Model 64620S Option 013: 100-channel Logic State/Software Analyzer (with overview)
Model 64620S Option 014: 120-channel Logic State/Software Analyzer (without overview)
Model 64630S 20-channel Logic State/Software Analyzer Probe Set
Model 64630S Option 010: 40-channel Logic State/Software Analyzer Probe Set
Model 64630S Option 011: 60-channel Logic State/Software Analyzer Probe Set
Model 64630S Option 012: 80-channel Logic State/Software Analyzer Probe Set
Model 64630S Option 013: 100-channel Logic State/Software Analyzer Probe Set
Model 64630S Option 014: 120-channel Logic State/Software Analyzer Probe Set
Model 64650A General Purpose Preprocessor
Model 64304A Emulation Bus Preprocessor
COMPONENTS
Model 64621A Logic State/Software Analyzer Control card
Model 64622A 40-channel Data Acquisition card (without overview)
Model 64623A 20-channel Data Acquisition card (with overview)
Model 64635A 20-channel Data Probe
Model 64636A 8-channel Clock Probe
Model 64962A 2-position Logic State/Software Analyzer Bus Cable
Model 64962A Option 001: 3-position Logic State/Software Analyzer Bus Cable
Model 64962A Option 002: 4-position Logic State/Software Analyzer Bus Cable

NOTE: When expanding an existing station to include another measurement system, IMB cables must be ordered separately. IMB cables are supplied on initial order of a complete development station with two or more subsystems.

Model 64964A 2-position Intermodule Bus Cable
Model 64964A Option 001: 4-position Intermodule Bus Cable
Model 64964A Option 002: 6-position Intermodule Bus Cable
Model 64964A Option 003: 8-position Intermodule Bus Cable
Model 64856AF User Definable Inverse Assembler on flexible disc
Model 64032A 16k Memory Expansion Module Card
(not required for Development Stations having serial number prefix 2309A or greater.)
Model 64620S+24D Logic State/Software Analyzer Training Course

Your Logic Instrumentation Field Engineer can help you determine the best configuration to meet your needs.

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